**Amendments to the Specification:**

Please replace the third paragraph on page 5, beginning at line 15 with the following amended paragraph:

Within the interior space 104 is a plurality of electron emitters 108 that face a storage medium 110. These electron emitters can, for example, comprise field (*i.e.*, tip) emitters as described in U.S. Patent No. 5,557,596 identified above. Alternatively, the electron emitters 108 can comprise flat emitters such as those described in U.S. Patent Application No. 09/836,124, filed April 16, 2001, which is hereby incorporated by reference into the present disclosure. As described in relation to FIG. 4, the storage medium 110 comprises a plurality of storage areas (not visible in FIGS. 1-3). In a preferred embodiment, each storage area of the storage medium 110 is responsible for storing one or more bits ~~more~~ of data. The electron emitters 108 are configured to emit electron beam currents toward the storage areas of the storage medium 110 when a predetermined potential difference is applied to the electron emitters. Depending upon the distance between the emitters 108 and the storage medium 110, the type of emitters, and the spot size (*i.e.*, bit size) required, electron optics may be useful in focusing the electron beams. Voltage is also applied to the storage medium 110 to accelerate the emitted electrons to aid in focusing the emitted electrons.

Please replace the second paragraph on page 8, beginning at line 7 with the following amended paragraph:

In a preferred embodiment, the electron emitters 108 are contained within a two-dimensional array comprising a plurality of emitters. By way of example, an array of 100 x 100 electron emitters 108 can be provided with an emitter pitch of approximately 5 to 100 micrometers in both the X and Y directions. As discussed above, each emitter 108 typically is used to access a plurality of storage areas of the storage medium 110. FIG. 4 provides a schematic representation of this relationship. In particular, this figure illustrates a single electron emitter 108 positioned above a plurality

of storage areas 400 of the storage medium 110. As indicated in FIG. 4, the storage areas 400, like the electron emitters 108, are contained in a two-dimensional array. In particular, the storage areas 400 are arranged in separate rows 402 and columns 404 on the surface of the storage medium 100. In a preferred ~~an~~ embodiment, each emitter 108 is only responsible for a portion of the entire length of predetermined numbers of rows 402. Accordingly, each emitter 108 normally can access a matrix of storage areas 400 of particular rows 402 and columns 404. Preferably, each row 402 that is accessed by a single electron emitter 108 is connected to a single external circuit.

Please replace the second paragraph on page 11, beginning at line 3 with the following amended paragraph:

In another reading approach, a diode structure is used to determine the state of the storage areas 400. According to this approach, the storage medium 110 is configured as a diode which can, for example, comprise a p-n junction, a ~~schottky,~~ Schottky barrier, or substantially any other type of electronic valve. FIG. 6 illustrates an example configuration of such a storage medium 110. It will be understood that alternative diode arrangements (such as those shown in U.S. ~~Pat.~~ Patent No. 5,557,596) are feasible. As indicated in this figure, the storage medium 110 is arranged as a diode having two layers 600 and 602. By way of example, one of the layers is p type and the other is n type. The storage medium 110 is connected to an external circuit 604 that reverse-biases the storage medium. With this arrangement, bits are stored by locally modifying the storage medium 110 in such a way that collection efficiency for minority carriers generated by a modified region 608 is different from that of an unmodified region 606. The collection efficiency for minority carriers can be defined as the fraction of minority carriers generated by the instant electrons that are swept across a diode junction 610 of the storage medium 110 when the medium is biased by the external circuit 604 to cause a signal current 612 to flow through the external circuit.